We claim:

　　1. A method for programming a group of at least one flash memory cell of an array, comprising:

　　A. performing a first pass of program verify and programming steps until each

5　flash memory cell of the group attains a threshold voltage that is at least X% of a program verify level but less than the program verify level; and

　　B. performing a second pass of program verify and programming steps until each flash memory cell of the group attains substantially the program verify level.

10　　2. The method of claim 1, wherein the step A comprises a loop of the following steps:

　　determining whether a flash memory cell of the group has not attained substantially X% of the program verify level, during the program verify step; and

　　generating a programming pulse for the flash memory cell of the group that has

15　not attained substantially X% of the program verify level, during the programming step.

　　3. The method of claim 1, wherein the step B comprises a loop of the following steps:

　　determining whether a flash memory cell of the group has not attained

20　substantially the program verify level, during the program verify step; and

　　generating a programming pulse for the flash memory cell of the group that has not attained the program verify level, during the programming step.

　　4. The method of claim 1, wherein the group includes a plurality of flash memory

25　cells to be programmed to multi-level threshold voltages, the method further comprising:

　　performing the first pass of program verify and programming steps until each flash memory cell of a first sub-group of the group attains a threshold voltage that is at least Y% of a first program verify level but less than the first program verify level, and until each flash memory cell of a second sub-group of the group attains a threshold voltage that

30　is at least Z% of a second program verify level but less than the second program verify level; and

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performing the second pass of program verify and programming steps until each flash memory cell of the first sub-group attains substantially the first program verify level, and until each flash memory cell of the second sub-group attains substantially the second program verify level.

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5. The method of claim 4, wherein (100%-Y%) of the first program verify level and (100%-Z%) of the second program verify level are each a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to a higher of the first and second program verify levels.

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6. The method of claim 1, wherein (100%-X%) of the program verify level is a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to the program verify level.

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7. The method of claim 1, wherein the at least one flash memory cell of the group is contained within a page of the array.

8. The method of claim 7, wherein the page of the array is situated between V_{ss} (source bias voltage) lines and between drain bit line junctions.

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9. The method of claim 1, further comprising:

storing a respective address of each flash memory cell of the group in a page buffer.

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10. A system for programming a group of at least one flash memory cell of an array, comprising:

means for performing a first pass of program verify and programming steps until each flash memory cell of the group attains a threshold voltage that is at least X% of a program verify level but less than the program verify level; and

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means for performing a second pass of program verify and programming steps until each flash memory cell of the group attains substantially the program verify level.

11. The system of claim 10, wherein the means for performing the first pass comprises:

means for determining whether a flash memory cell of the group has not attained substantially X% of the program verify level, during the program verify step; and

5   means for generating a programming pulse for the flash memory cell of the group that has not attained substantially X% of the program verify level, during the programming step.

12. The system of claim 10, wherein the means for performing the second pass
10   comprises:

means for determining whether a flash memory cell of the group has not attained substantially the program verify level, during the program verify step; and

means for generating a programming pulse for the flash memory cell of the group that has not attained the program verify level, during the programming step.
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13. The system of claim 10, wherein the group includes a plurality of flash memory cells to be programmed to multi-level threshold voltages, the system further comprising:

means for performing the first pass of program verify and programming steps until
20   each flash memory cell of a first sub-group of the group attains a threshold voltage that is at least Y% of a first program verify level but less than the first program verify level, and until each flash memory cell of a second sub-group of the group attains a threshold voltage that is at least Z% of a second program verify level but less than the second program verify level; and

25   means for performing the second pass of program verify and programming steps until each flash memory cell of the first sub-group attains substantially the first program verify level, and until each flash memory cell of the second sub-group attains substantially the second program verify level.

30   14. The system of claim 13, wherein (100%-Y%) of the first program verify level and (100%-Z%) of the second program verify level are each a maximum potential change

to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to a higher of the first and second program verify levels.

15. The system of claim 10, wherein (100%-X%) of the program verify level is a maximum potential change to a threshold voltage of a flash memory cell from programming any adjacent flash memory cells to the program verify level.

16. The system of claim 10, wherein the at least one flash memory cell of the group is contained within a page of the array.

17. The system of claim 16, wherein the page of the array is situated between V_{ss} (source bias voltage) lines and between drain bit line junctions.

18. The system of claim 10, further comprising:

a page buffer for storing a respective address of each flash memory cell of the group.